1. A system comprising:

a digital signal processor comprising a bus connectable to a memory; and

a butterfly coprocessor connected to the bus, wherein the butterfly coprocessor performs an operation scheduled by the digital signal processor.

2. The system of claim 1, wherein the digital signal processor further comprises:

a data address generator coupled to the bus, wherein the data address generator addresses the memory on behalf of a requesting device.

3. The system of claim 2, wherein the digital signal processor further comprises an arithmetic unit for performing arithmetic operations in the digital signal processor.

4. The system of claim 3, wherein the arithmetic unit further comprises a branch metric unit for performing branch metric calculations.

5. The system of claim 4, wherein the arithmetic unit further comprises one or more registers to which the branch metric unit may store one or more results.

6. The system of claim 5, wherein the data address register may address one or more registers in the arithmetic unit.

7. The system of claim 1, wherein the butterfly coprocessor further includes a plurality of butterfly units for performing butterfly operations.

8. The system of claim 7, wherein the butterfly operations are parallel operations.

9. The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor further perform add-compare-select operations at the direction of the digital signal processor.

10. The system of claim 8, wherein the plurality of butterfly units in the butterfly coprocessor further perform approximations of log sum exponential operations at the direction of the digital signal processor.

11. The system of claim 8, wherein a path metric retrieved from a path metric memory is accessed by the data address generator of the digital signal processor.

12. The system of claim 11, wherein the data address generator of the digital signal processor further retrieves a branch metric from the branch metric unit.

13. A method comprising:

identifying a stage of a trellis diagram;

calculating branch metrics for each node of the stage; and

simultaneously computing two or more path metrics for the stage based upon the branch metrics.

14. The method of claim 13, further comprising:

storing the path metrics in a memory.

15. The method of claim 13, calculating the branch metrics for each node of the stage further comprising:

identifying a number of nodes in the stage;

identifying a number of branches extending from each node; and

calculating a branch metric for each branch.

16. The method of claim 14, simultaneously computing two or more path metrics for the stage based upon the branch metrics further comprising:

identifying a node of the stage;

retrieving a prior path metric from the memory, wherein the prior path metric leads to the node;

identifying a number of branches extending from the node in the stage; and

allocating a butterfly unit for each branch extending from the node, wherein the butterfly unit calculates a new path metric from the prior path metric and the branch metric.

17. A method comprising:

receiving a request to decode a bit stream, wherein the bit stream was encoded by an encoder and the encoder is described using a trellis diagram;

identify a stage of the trellis diagram;

compute branch metrics for all nodes of the stage;

retrieve path metrics for a different stage of the trellis diagram from a memory; and

simultaneously calculate new path metrics for each node of the stage.

18. The method of claim 17, further comprising:

storing the new path metrics for each node of the stage in the memory; and

identify a new stage of the trellis diagram.

19. An article comprising a medium storing a software program which, when executed, causes a processor-based system to:

identify a stage of a trellis diagram;

calculate branch metrics for each node of the stage; and

simultaneously compute two or more path metrics for the stage based upon the branch metrics.

20. The article of claim 19, further storing a software program which, when executed, causes a processor-based system to store the path metrics in a memory.

21. A system comprising:

a digital signal processor, comprising:

a bus connectable to a memory;

a data address generator and

an arithmetic unit; and

a butterfly coprocessor connected to the bus, wherein the butterfly coprocessor performs an operation scheduled by the digital signal processor.

22. The system of claim 21, wherein the digital signal processor further comprises a software program which, upon execution:

identifies a stage of a trellis diagram;

identifies a number of nodes in the stage; and

identifies a number of branches extending from each node.

23. The system of claim 22, wherein the butterfly coprocessor further comprises a plurality of butterfly units.

24. The system of claim 23, wherein the number of butterfly units equals the number of nodes in the stage.

25. The system of claim 24, wherein the operation performed by the butterfly coprocessor comprises computing path metrics for the stage.

26. The system of claim 25, wherein the butterfly units simultaneously compute a path metric for each node of the stage.